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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,397	10/01/2003	Tadayoshi Ueda	R2180.0181/P181	4415

24998 7590 06/19/2006

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EXAMINER	
RAHMAN, FAHMIDA	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,397	UEDA, TADAYOSHI	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4* is/are rejected.

7)☒ Claim(s) *2 and 3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to communications filed on 4/03/2006.

2. Claims 2 and 3 have been amended, no new claims have been added, no claims have been canceled. Thus, claims 1-4 are pending.

3. Applicants arguments are moot in view of new grounds of rejections.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohmae (US patent 5237698).

For claim 1, Ohmae teaches the following limitations:

A power supply system for supplying power to a CPU (Fig 1), said power supply system comprising: a power supply circuit for supplying the CPU with a prescribed supply voltage (8); a voltage detecting circuit (5) for outputting a reset signal for resetting the CPU when the supply voltage is below a prescribed voltage detection value (CPU is conditionally reset when it is not in operation mode. The CPU "operation mode" voltage level mentioned in line 58 of column 1 can be equated with the limitation "prescribed voltage detection value". Reset circuit 5 outputs reset signal when the supply voltage is

below initial reset value, which is definitely lower than CPU operation mode voltage level, or prescribed voltage detection value. Therefore, Ohmae teaches the limitation that a voltage detecting circuit 5 outputs a reset signal 12 for resetting CPU, when supply voltage VCC is lower than prescribed voltage detection value 5V);

a control circuit for decreasing the supply voltage to a prescribed power save voltage level when a power saving mode is set ("standby mode" where power save voltage is 3V), wherein said control circuit decreases the supply voltage to be the prescribed power save voltage level after decreasing the prescribed voltage detection value to be less than or equal to the power save voltage level when the power saving mode is set (lines 18-24 of column 2 mention that processor switches from operation mode or 5V voltage requirement to standby mode so that supply voltage may be reduced during the standby mode. Thus, the prescribed voltage detection value is changed from operation mode to standby mode. CPU enters into the standby mode first and then supply voltage is reduced to power save voltage level. Thus, supply voltage is reduced to the prescribed power save voltage 3V after CPU enters into standby mode or decreasing the prescribed voltage detection value from 5V CPU operating mode to 3V or less standby mode CPU voltage), and wherein said control circuit recovers the prescribed voltage detection value after recovering the supply voltage when the power saving mode is terminated (when the power saving mode is terminated and operation mode is set, CPU can't have the operation mode voltage unless power supply produces enough

voltage. Thus, power supply voltage is recovered first and the prescribed detection value or operation mode voltage is recovered next)

For claim 4, Ohmae teaches the following limitations:

A method for supplying power to a CPU providing a power saving mode (Fig 1), said method comprising the steps of:

providing a reset signal for resetting the CPU when an output voltage from a power supply is less than or equal to a prescribed operable level (CPU is conditionally reset when it is not in operation mode. The CPU "operation mode" voltage level mentioned in line 58 of column 1 can be equated with the limitation "prescribed operable level". Reset circuit 5 outputs reset signal when the supply voltage is below initial reset value, which is definitely lower than CPU operation mode voltage level, or prescribed operable level. Therefore, Ohmae teaches the limitation that a voltage detecting circuit 5 outputs a reset signal 12 for resetting CPU, when supply voltage VCC is lower than prescribed operable level 5V);

setting a power saving mode ("standby mode" or low voltage mode);

decreasing the prescribed operable level before decreasing the output voltage down to a power saving level (lines 18-24 of column 2 mention that processor switches from operation mode or 5V voltage requirement to standby mode so that supply voltage may be reduced during the standby mode. Thus, the prescribed operable level is changed from operation mode voltage to standby mode voltage. CPU enters into the standby mode first and then supply voltage is reduced to power save voltage level. Thus, supply

voltage is reduced to the power saving level 3V after CPU enters into standby mode or after decreasing the prescribed operable level from 5V CPU operating mode voltage to 3V or less CPU standby mode voltage);

resetting the power saving mode ("operation mode");

and recovering the prescribed operable level (the level required to maintain operation mode of CPU) after recovering the output voltage (the power supply output voltage is further reduced from 3V to 2V or lower for battery replacement. After the battery replacement, the output voltage of power supply can increase to 3V while staying within standby mode. Thus, the output voltage is recovered from 2V or lower to 3V in standby mode, which happens before recovering the prescribed operable level of operation mode of CPU. Thus, Ohmae teaches the limitations recovering the prescribed operable level after recovering the output voltage).

Allowable Subject Matter

Claims 2 and 3 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

JAMES TRUJILLO
PATENT EXAMINER
TC 2100